A Class-C Self-Mixing-VCO Architecture with High Tuning-Range and Low Phase-Noise for mm-Wave Applications

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Abstract—Achieving high tuning-range and low phase-noise simultaneously in mm-wave voltage-controlled oscillators (VCO) has been challenging. Our architecture, referred herein as a self-mixing VCO (SMV), utilizes a Class-C push-push VCO topology to generate the first ($f_0$) and second harmonics ($2f_0$) and then mixes them together to obtain the desired third harmonic ($3f_0$) component. Compared to a fundamental-mode VCO operating at $3f_0$ in mm-wave band, the SMV architecture achieves superior frequency tuning range (FTR) and phase-noise (PN) performance. A Class-C VCO topology enhances the second-harmonic content to improve mixing efficiency, decreases parasitic capacitance and reduces phase noise. A 52.8- to 62.5 GHz SMV prototype is designed and implemented in a 0.13-μm CMOS process. Measurement results show an FTR of 16.8% together with a PN of −190.85 dBc/Hz at 1 MHz offset – resulting in an FTR-inclusive figure-of-merit (FOMT) of -100.57 dBc/Hz at 1 MHz offset from a 1.2V supply voltage.

Index Terms— Self-Mixing-VCO, SMV, low phase noise, high tuning range, Class-C, mm-wave, 60-GHz.

I. INTRODUCTION

The deployment of mm-wave portion of frequency spectrum for wireless communication is gaining tremendous popularity. The availability of wide bandwidth at these bands make them attractive for high-data-rate applications such as wireless high-definition video streaming and medical imaging [1]–[3]. One of the key challenges in most communication systems operating at 60 GHz band and beyond is synthesis of on-chip LO frequency – with high spectral purity, and large tuning range to mitigate the effect of variations. The signal synthesis techniques can be broadly classified into direct and indirect synthesis, based on whether the desired LO frequency is same as the VCO fundamental ($f_0$), or higher than $f_0$, respectively. A good comparison between these techniques has been presented in [3].

At mm-wave frequencies, direct LO synthesis techniques face several design challenges to meet phase noise and tuning range requirement. First, as $f_0$ approaches the maximum oscillation frequency ($f_{max}$) of the device, the available power gain of transistors degrades. Thus, an excess power is required to guarantee the oscillation start-up. Second, the low quality factor (Q) of passive devices (varactors and inductors) implemented on silicon substrate adversely impacts the phase noise performance. Third, the parasitic capacitance of the oscillator active core, interconnects, and buffer stage ($C_{par}$) become a significant fraction of the total tank capacitance, thereby permitting only a small MOS varactor ($C_{var}$) to be used. FTR, being proportional to $C_{var}$ and inversely proportional to $C_{par}$, is therefore significantly limited [1]–[2]. Fourth, the switched-tuning technique [4] is no longer effective for reducing $K_{VCO}$, since switches add more parasitic capacitance and loss to the tank. Consequently, the voltage-noise on the oscillator control line with a large $K_{VCO}$ results in increased amplitude-noise to phase-noise conversion [4].

Indirect LO synthesis techniques generate and utilize higher-order harmonics to enhance the FTR. Fig. 1(a) shows a triple-push-VCO structure [2] where $f_0$ and $3f_0$ generated by three VCOs are added destructively and constructively, respectively. Although achieving a wide FTR at 60 GHz in [2], extensive electromagnetic simulations of the nested-inductor and tank layouts are needed and any error in coupling factors may alter the centre frequency, degrade the Q and adversely affect the phase noise. Furthermore, improving the phase noise requires higher selectivity at $f_0$, thereby reducing the power of the desired $3f_0$ harmonic. Finally, due to the use of multiple oscillators, a relatively large DC power is consumed. Fig. 1(b) shows another technique [5] where $f_0$ and $3f_0$ generated by the VCO is suppressed and amplified, respectively, by a non-linear buffer resonant at $3f_0$. This technique however, suffers from
a trade off of output power at $3f_0$ with the DC power consumption in the non-linear buffer.

In this paper, we present a self-mixing-VCO (SMV), whose basic topology is shown in Fig.1(c). Instead of using the $3f_0$ component of the VCO, the SMV utilizes the $2^{nd}$ harmonic ($2f_0$) from the common-mode output along with the fundamental ($f_0$) from the differential output. The amplitude of $2f_0$ can be extracted from a VCO with a larger amplitude than $f_0$, thereby making it a superior implementation than [5] and [2]. Furthermore, the SMV architecture does not suffer from strict matching requirements, single-ended operation and large power consumption of triple push VCO [2]. Finally, we propose the use of a Class-C VCO topology to further enhance the $2f_0$ component and improve the phase noise. Thus, the specifications for a low phase noise, large tuning range and low DC power consumption can be simultaneously achieved.

The paper is organized as follows: Section II describes the Class-C SMV architecture in detail. Section III presents the measurement results of a proof-of-concept prototype SMV that is implemented in a 0.13-µm CMOS process as well as performance comparison with the state-of-the-art designs. Section IV provides some concluding remarks.

II. CLASS-C SMV ARCHITECTURE

A simplified schematic diagram of the SMV is shown in Fig. 2(a). In the first stage, the structure uses a class-C push-push VCO to generate $f_0$ and $2f_0$ components at 20 GHz and 40 GHz, respectively. Operating the VCO core at 20 GHz instead of 60 GHz ensures easier start-up owing to larger $g_{m}$ of transistors operating at a lower fraction of $f_{max}$, and higher Q of varactor and inductors. For example, a 200 pH symmetric spiral inductor in the 0.13-µm CMOS process used herein has a Q of 25 and 8 at 20 GHz and 60 GHz, respectively. Higher Q, lower $C_{par}$ and $K_{VCO}$ also improve the FTR and phase noise performance, as discussed in the previous section.

In the second stage, a single-balanced active mixer is used to combine the $f_0$ and $2f_0$ components and generate a desired LO component at $3f_0$ (~60 GHz) at the output of the mixer. An active mixer is preferred due to its conversion gain in comparison to a passive mixer [6]. A $\lambda/4$ transmission-line is used for biasing the VCO and mixer as well as to maximize the $2^{nd}$ harmonic component. This $\lambda/4$ line is ideally open (high impedance) at $2f_0$ and allows the second harmonic current $I_{3f_0}$ to sink into the mixer. The mixer is tuned at $3f_0$ (~60 GHz) to provide frequency selectivity and suppress spurious components and lower mixing-sideband.

Next, we discuss the merits of a class-C VCO over the class-B cross-coupled VCO for the SMV architecture.

A. Benefits of Using Class-C Push-Push VCO

Practical implementation of the SMV substantially benefits from efficient generation of a strong $2f_0$ component; otherwise, the generated $3f_0$ signal at the output of the mixer will have a low amplitude and the mixer may require a higher power consumption to increase its conversion gain.

The class-B push-push VCO has been frequently used for generating $2f_0$ [7]. However, it achieves low DC-to-$2f_0$ efficiency due to the nature of the VCO current waveform. Fig. 2(b) shows a class-B cross-coupled VCO, with $V_{Bias-Gate} = V_{DD}$, where the cross-coupled transistors ($M_1$ and $M_2$) act as switches and operate mostly in triode region. In contrast, in a class-C design, with $V_{Bias-Gate} < V_{DD}$, these transistors operate in the saturation region mostly when conducting. Thus, in comparison to the ideal class-B operation with square-wave drain current, class-C operation leads to an impulse-like waveform with reduced conduction angle, $\phi_L$. This has two main benefits: first, while the square-wave drain current has a zero $2^{nd}$-order harmonic in ideal class-B operation...
(although in a real implementation, the current waveform is not an ideal square-waveform and contains some 2\(^{nd}\) harmonic), the impulse-shape drain-current in class-C results in generating a larger 1\(^{st}\) and 2\(^{nd}\) harmonic and consequently higher DC-to-\(f_0\) and DC-to-2\(f_0\) efficiencies. Second, as proven in [8], class-C drain current waveform in VCOs results in 3.9 dB lower phase noise at same DC power consumption (or 36% lower DC power consumption while achieving the same phase noise).

In addition to having a better DC-to-2\(f_0\) efficiency and superior phase noise performance, the class-C VCO has a lower parasitic capacitance, \(C_{\text{D,Par}}\), across the resonator LC-tank. Fig. 3 compares the drain capacitance, \(C_{\text{D,Par}}\), for class-C and class-B VCOs with the same transistor size. As can be seen, \(C_{\text{D,Par}}\) in class-C is almost 2/3\(^{rd}\) of that of class-B. This is owing to the fact that the class-C cross-coupled transistor operates in the saturation region. Thus, a class-C VCO operation also ensures a higher FTR, especially at mm-wave frequency.

![Fig. 3. Parasitic capacitance (\(C_{\text{D,Par}}\)) of cross-coupled pair in Class-B and Class-C VCO.](image)

III. IMPLEMENTATION AND MEASUREMENT RESULTS

As a proof-of-concept, the SMV shown in Fig. 2(a) is designed and implemented in a 0.13-\(\mu\)m CMOS process. Fig. 4 shows its die micrograph. Active die area (excluding pads) is about 300\(\times\)670 \(\mu\)m\(^2\). The core class-C VCO is designed to operate between 17-to-21 GHz; the mixer and the output buffer at 60 GHz. The output buffer is designed to drive the 50-\(\Omega\) load of the test equipment. The VCO varactor is implemented using a thick oxide MOS capacitor. Both \(L_{\text{Bias}}\) and \(L_B\) are implemented using a \(\lambda/4\) transmission-line. All transmission-lines and inductors are simulated using Momentum planar 3D electromagnetic software.

The DUT is directly measured using a signal and spectrum analyser (R&S-FSW67). Fig. 5 shows the output spectrum of SMV at 62.48 GHz with the signal power of -31 dBm. Fig. 6 shows the phase-noise plot of SMV at 53.68 GHz with a PN of -100.57 dBc/Hz at 1 MHz and -124.75 dBc/Hz at 10 MHz offset, respectively. Fig. 7 shows the tuning range plot of SMV, spanning from 52.8-to-62.5 GHz with an FTR of 16.8%.

Table I summarizes the performance of the Class-C SMV prototype as well as compares it to other state-of-the-art designs. Two popular figures of merit (FOMs) for comparing VCOs are:

\[
FOM = PN - 20\log(f_0/\Delta f) + 10\log(P_D/1mW)
\]

\[
FOM_T = FOM - 20\log(FTR/10)
\]

Based on Table I, the performance of the Class-C SMV compares favourably with state-of-the-art.

![Fig. 4. Chip micrograph of SMV architecture](image)

![Fig. 5. Buffered Output Spectrum at 62.48 GHz](image)
TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

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<td>Architecture</td>
<td>Class-C Self-Mixing VCO(SMV)</td>
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<td>Class-B Inductive peaking</td>
<td>Standing-Wave VCO</td>
<td>Dual Mode Inductive Divider Feedback</td>
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<td>Frequency (GHz)</td>
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<td>-89.5</td>
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<td>PN (dBc/Hz) @ 10 MHz</td>
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<td>P_{dc} (mW)*</td>
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<td>Buffered P_{out} (dBm)</td>
<td>-31@62GHz, -28@52.8 GHz</td>
<td>-36.4@63.2 GHz</td>
<td>-20@64GHz</td>
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<td>-38@56.9 GHz, -31@75GHz</td>
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<td>FOM (dBc/Hz)</td>
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<td>FOM_{t} (dBc/Hz)</td>
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* Power consumption does not include buffers.

IV. CONCLUSION

A low phase-noise, and high tuning-range self-mixing-VCO architecture is described for mm-wave applications. A 60 GHz-band proof-of-concept prototype is designed and measured in a 0.13-μm CMOS process. The structure uses a push-push class-C VCO for low phase noise, high tuning range, and higher first and second harmonic content, and then mixes these two harmonics to generate the third harmonic as the desired output. This indirect synthesis has superior tuning range and phase noise compared to direct synthesis techniques. The implemented 60 GHz prototype compares favourably with the state-of-the-art (employing direct or indirect synthesis) and achieves the best reported FOM_{t} as per our knowledge.

ACKNOWLEDGMENT

Dr. H. Djahanshahi (PMC-Sierra) for his technical assistance and fruitful discussions, R. Mehrabi for CAD tools assistance, Dr. R. Rosales for technical help and Rohde & Schwarz for providing measurement equipment.

REFERENCES


Fig. 6. Measured phase noise at 53.68 GHz

Fig. 7. Measured frequency tuning range